DDR SDRAM DIMM

D40PB12C – 512MB

For the latest data sheet, please visit the Super Talent Electronics web site: www.supertalentmemory.com

Features

- Power supply : Vdd: 2.6V ± 0.1V, Vddq: 2.6V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- High Performance Heat Spreader
- PCB : Height 1.250" (31.75mm), double sided component

Description

This document describes Super Talent Electronics' 64M x 64-bit (512MB) DDR500 SDRAM (Synchronous DRAM) CL3 memory module. The components on this module include sixteen 32M x 8-bit DDR500 SDRAM in TSOP packages. This 184-pin DIMM uses gold contact fingers and requires +2.6V.

Figure 1: Module with Heat Spreader

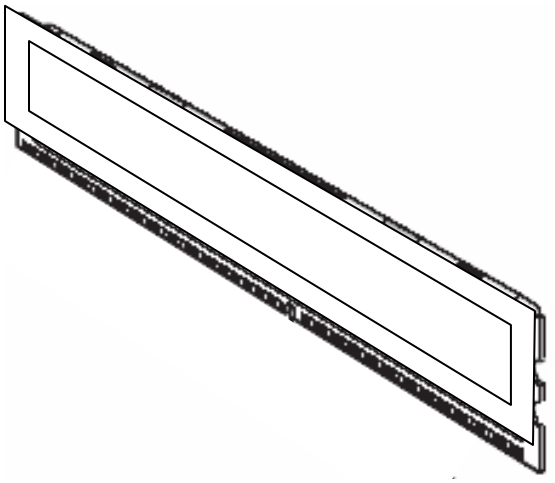
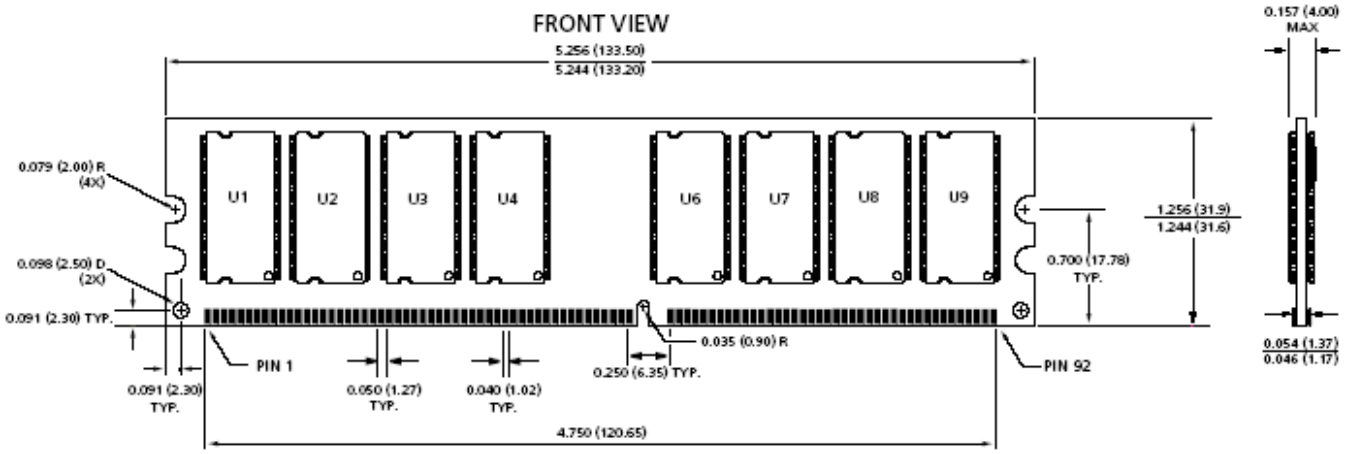
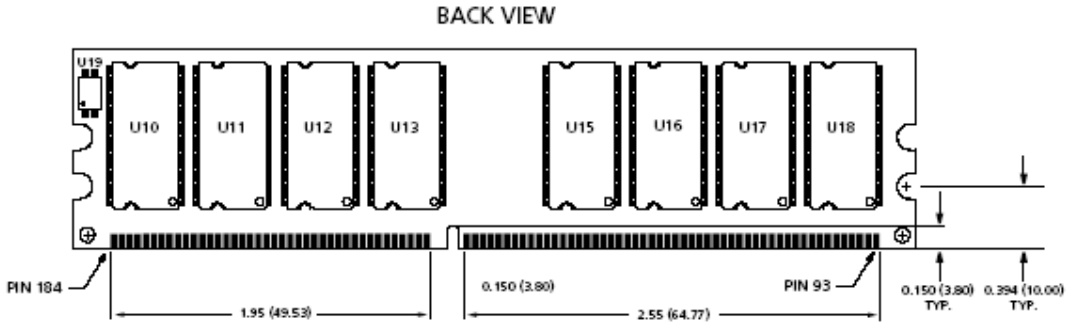


Figure 2: 184-Pin DIMM Dimensions – under heat spreader





NOTE:

All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

